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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/244,798	02/05/99	PARIKH	S 002818/PDD/P

EXAMINER	
PHAM, T	
ART UNIT	**PAPER NUMBER**
2813	#16

MM91/1018

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DATE MAILED: 10/18/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/244,788	Applicant(s) PARIKH, SUKETU A.	
	Examiner Thanhha Pham	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2001 and 08 August 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-19,21 and 23-42* is/are pending in the application.

4a) Of the above claim(s) *33-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-19,21 and 23-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *15* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. This application contains claim33-42 drawn to an invention nonelected with traverse in Paper No. 9. A complete reply to the final rejection must include cancelation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 11 ,

line 2, "the trench" lacks of antecedent basis. It is not clear that the second trench or the first trench is filled with a conductive material.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1, 5, 7-9, 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Inohara et al [US 5,976,972].

Inohara et al, figs 8-49 col 1-19 particularly embodiment of figs 28-32, discloses the claimed method of forming a structure on a substrate comprising steps of:

depositing a first dielectric layer (43, Silicon oxide containing C, fig 28) on a substrate;

depositing a second dielectric layer (44, SiN, fig 28) on the first dielectric layer;

depositing a first mask layer on the second dielectric layer wherein the first mask layer including a first via pattern having a width T, anisotropically etching the first via pattern (51, fig 28) through the second dielectric layer, and removing the first mask layer [see col 13 lines 20-24 for details]

depositing a third dielectric layer (45, Silicon oxide containing C, fig 29) on the second dielectric layer;

depositing a second mask (47, fig 29) on the third dielectric layer wherein the second mask includes a trench pattern overlaying the first via pattern and having a width P, such that T exceeds P by a measure M, whereby the first via pattern;

anisotropically etching the trench pattern through the third dielectric layer thereby forming a first trench and a second via pattern in the third dielectric layer;

anisotropically etching the second via pattern through the first dielectric layer thereby forming a via hole extending to a substrate;

anisotropically etching the first trench through the second dielectric layer thereby forming a second trench extending through the second and third dielectric layers, wherein the via hole and the second trench are adapted for fabricating a dual damascene structure; [see figs 30-31 col 13 lines 39-53]; and

filling the second trench and the via hole with a conductive material (49, Al-Cu, fig 32) (491-492, fig 32) whereby the dual damascene is formed.

4. Claims 13-14, 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Inohara et al [US 5,976,972].

** Notice: *With respect to claim 14, interpreting the claim under a broad scope, rejection is based on the scope that forming the first trench at a distance D from the second trench and forming the sacrificial etch segment at a width W, such that D exceeds W by a measure N, the measure N is chosen to be zero.*

Innohara et al, figs 35-40 col 1-19 particularly col 14 lines 30-67 and col 15, discloses the claimed method of forming a structure on a substrate comprising steps:

forming a dielectric stack (54, 43, 44, fig 37) including an etchstop layer (44, SiN); depositing a first mask layer (56, fig 38) on the etchstop layer wherein the first mask includes: a first via pattern, a second via pattern and a sacrificial etch pattern wherein the sacrificial patterned are positioned between the first and second via patterns such that the sacrificial pattern has a width W [see fig 38, the first via pattern, the sacrificial pattern and the second via pattern are defined by the first mask (56, fig 38) in a way such that the first via pattern, the sacrificial pattern and the second via pattern are adjacent to each other, wherein the first and second via patterns are to form first and second conductive plugs (491, fig 40) separated to

each other by the sacrificial etch segment in the split (51, figs 39-40) in the etch stop (44, fig 39-40)];

anisotropically etching the first and second via patterns through the etchstop layer and forming a sacrificial etch segment by anisotropically etching the sacrificial pattern through the etchstop layer [see fig 39, the first via pattern, the sacrificial pattern and the second via pattern are included in the split (51, fig 39) by anisotropically etching through the etchstop (44, fig 39) in the way such that the first and second via patterns are to form the conductive plugs (491, fig 40), the sacrificial pattern is to form the sacrificial etch segment defined between the conductive plugs (491. figs 39-40) in the split (51, fig 39)];

forming first and second trenches (trenches for forming upper wiring elements 492, fig 40) on the etchstop layer (44) such that the first and second trenches do not overlay the sacrificial etch segment and the sacrificial etch segment is positioned between the first and second trenches (fig 40);

forming a first via underlying the first trench such that the first via hole communicates with the first trench;

forming a second via hole underlying the second trench such that the second via hole communicates with the second trench, wherein: (1) the first trench & the first via hole and (2) the second trench & the second via hole are adapted for forming a first dual damascene structure and a second dual damascene structure respectively;

[see fig 40]

filling the first and second trenches, and the first and second via holes with conductive material (49, Al-Cu, fig 40) whereby the first and second dual damascene structure are formed.

5. Claims 13-14 and 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin [US 6,093,632].

Liu et al, figs 4-8 and col 1-6, discloses the claimed method of forming a structure on a substrate comprising steps:

forming a dielectric stack (3,4,10a, fig 4) including an etchstop layer (10a, SiN); depositing a first mask layer (11, fig 5) on the etchstop layer wherein the first mask includes: 1) a first via pattern, 2) a second via pattern and 3) a sacrificial etch pattern wherein the sacrificial patterned are positioned between the first and second via patterns such that the sacrificial pattern has a width W [see fig 5, the first and second via patterns are defined in the first mask 11 for etching the etchstop layer at positions overlaying the interconnect structures 2 to make a dual damascene structure in following step, and the sacrificial etch pattern is defined in the first mask 11 for etching the etchstop layer at position not overlaying the interconnect structure 2 for reduced insulator capacitance by reducing areas of the etchstop layer 10a];

anisotropically etching the first and second via patterns through the etchstop layer and forming a sacrificial etch segment (12a not overlaying the interconnect structure 2, fig 5) by anisotropically etching the sacrificial pattern through the etchstop layer;

forming a first trench (15b, fig 7) on the etchstop layer such that the first trench does not overlay the sacrificial etch segment;

forming a second trench (15b, fig 7) on the etchstop layer such that 1) the second trench does not overlay the sacrificial etch segment and 2) the sacrificial etch segment is positioned between the first and second trenches;

forming a first via hole (12b, fig 7) underlying the first trench such that the first via hole communicates with the first trench;

forming a second via hole (12b, fig 7) underlying the second trench such that the second via hole communicates with the second trench, wherein: 1) the first trench & the first via hole and 2) the second trench & the second via hole are adapted for forming a first dual damascene structure and a second dual damascene structure respectively;

filling the first and second trenches, and the first and second via holes with conductive material (e.g. Cu, fig 8) whereby the first and second dual damascene structure are formed.

With respect to claim 14, see fig 6-8, Lin teaches forming the first trench at a distance D from the second trench and forming the sacrificial etch segment at a width W such that D exceeds W by a measure N.

4. Claims 19, 21, 23 and 28-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin [US 6,093,632].

Lin, figs 4-8 col 1-6, discloses the claimed method of forming a structure on a substrate comprising steps of:

depositing a first dielectric (4, silicon oxide, fig 4) on a substrate wherein a cap layer (3, fig 4) interposed between the substrate and the first dielectric layer;

depositing a second dielectric layer (10a, SiN, fig 4) on the first dielectric layer;

depositing a first mask layer (11, fig 5) on the second dielectric layer wherein the first mask layer includes: (1) a first via pattern having a width T, (2) a second via pattern and (3) a sacrificial etch pattern position between the first and second via patterns such that the sacrificial etch pattern has a width W;

anisotropically etching the first and second via patterns through the second dielectric layer and forming a sacrificial etch segment by simultaneously anisotropically etching the sacrificial etch pattern through the second dielectric layer [see fig 5-6];

removing the first mask layer;

depositing a third dielectric layer (13, silicon oxide, 6) on the second dielectric layer;

depositing a second mask layer (14, fig 6) on the third dielectric layer, wherein the second mask layer includes: (1) a first trench pattern with a width P overlaying the first via pattern and the third dielectric layer , and (2) a second trench pattern overlaying the second via pattern and the third dielectric layer, and having a distance D between the first and second trench patterns wherein D exceed W by a measure N;

anisotropically etching the first and second trench patterns through the third dielectric layer thereby forming a first trench and a second trench, additionally forming a third and fourth via pattern;

anisotropically etching the third and fourth via patterns through the first dielectric layer thereby forming a first via hole and a second via hole, , in which: 1) the first trench and the first via hole are adapted for forming a first dual damascene structure and 2) the second trench and the second via hole are adapted for forming a second dual damascene structure;
[see figs 6-7, col 5 lines 54-67 and col 6 lines 1-8]; and

filling the first trench, the first via hole, the second trench and the second via hole with conductive material (Cu, fig 8) whereby the first and second dual damascene structures are formed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 6, 7-8, 10, 14-15, 24-27 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin [US 6,093,632] in the view of Inohara et al [US 5,976,972].

With respect to claim 31, Lin fails to teach the width T of the first via pattern exceeding the width P of the first trench pattern by a measure M.

However, Inohara et al teaches that forming a dual damascene structure with the width T of the first via pattern exceeding the width P of the first trench pattern by a measure M will provide better connection (communication) between the first trench and the first via hole in interconnect -- since an allowance for an alignment error between upper and lower wiring elements (in the first trench and the first via hole respectively) is provided thereby the area

contact between the upper and lower wirings is not deteriorate due to misalignment [see Inohara et al col 12 lines 60-67 and col 13 lines 1-3].

Therefore, it would have been obvious for those skilled in the art to combine the teaching of Inohara et al in the process of Lin to make the width T of the first via pattern exceeding the width P of the first trench pattern by a measure M for making a better dual damascene structure with reasons given above.

With respect to claims 7, 10, 25 and 27, amorphous fluorinated carbon, organic SOG, SOG, aero-gel, polyarylene ethers, fluorinated polyarylene ether, divinyl siloxane benzocyclobutane, and Black DiamondTM are well-known low-k dielectric materials. It would have been obvious for those skilled in the art to use any of these material in the process of Lin and/or Inohara et al to make a dual damascene structure - since it has been well-known in the art that these materials can provide a good dual damascene structure with a decreased capacitance for a better interconnection in a semiconductor device.

With respect to claims 6, 14-15, 24 and 32, ranges values of measure M and measure N are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges

are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ233, 255 (CCPA). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time of invention was made would have used any suitable range of N or M in the process of Lin and/or Inohara et al in order to optimize the process.

Response to Arguments

7. Applicant's arguments filed 06/29/01 have been fully considered but they are not persuasive.

Regarding to applicant's argument on pages 7-8 that "applicant sequentially forms first and second dielectric layer on a substrate without interposing a cap layer between the first dielectric and the substrate" and Inohara et al teaches "forms the via hole through the first dielectric layer and the cap layer" while "applicant's via hole that extends to the substrate is not formed through a cap layer", the argument is not persuasive because the claim language does not excluding the step of forming a cap layer (claim 1 uses "the method comprising").

Rejection, therefore, is still proper. Morever, forming or not forming a cap layer depending on the design choice of a structure on a substrate is obvious for those skilled in the art.

Regarding to applicant's argument on pages 9-11, contrary to applicant's argument, Lin teaches forming a first mask having first and second via patterns for forming first and second via holes in the first dielectric layer where first and second dual damascene structures are formed in subsequent steps (figs 7-8) and a sacrificial etch pattern for removing portions of etchstop/second dielectric layer to reduce insulator capacitance. Applicant's attention is respectfully directed figure 5 where the first mask 11 includes: **1)** the first and second via patterns (12a, fig 5, col 5 lines 9-16, lines 34-43) overlaying interconnect structures (2, fig 5) for forming the first and second via holes (12b, figs 6-7, col 5 lines 59-61) in the first dielectric layer (4, fig 7); and 2) the sacrificial pattern (12a, fig 5) for removing the second dielectric/etchstop layer at portions not for forming dual damascene structure (not overlaying the interconnect structures 2) to reduce insulator capacitance (col 5 lines 14-16).

Regarding to applicant's argument on pages 12-13, as explained above, Lin does disclose "a first via pattern" in the first mask 11 to form the first via hole 12b in the first dielectric layer 4: first, the second dielectric/etchstop layer 10a being etched through the first mask 11 to form a via opening 12a in the second dielectric/etchstop layer; and then the first dielectric layer 4 being etched through the opening via opening 12a (between the second dielectric/etchstop layer as a mask) to form the first via hole 12b which communicates with the first trench 15b to create the dual damascene structure. Lin also discloses the sacrificial etch segment being formed when the second dielectric/etchstop layer 10a being etched through the sacrificial etch pattern located that does not overlay the interconnect structures 2 and in the

mask 11 (see figs 4-5) - the sacrificial etch pattern is positioned between the first and second via patterns wherein the first and second via patterns overlay the interconnect structures 2. The combination of Inohara et al and Lin would result in the steps that are employed in forming the claimed structure.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (703) 308-6172. The examiner can normally be reached on Monday-Thursday 8:00 AM - 7:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bowers Charles can be reached on (703) 308-2417. The fax phone numbers for

the organization where this application or proceeding is assigned are (703) 308-3432 for regular communications and (703) 308-7725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thanhha Pham
Monday, October 15, 2001

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800